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sealing the front surface of a wafer having the front and rear surfaces and having formed a plurality of semiconductor chips on the front surface with resin material;

a first marking the position information corresponding to each chip in the region of each chip at the rear surface of said wafer;

conducting electrical test to each chip;

a second marking the result of said electrical test corresponding to each chip in the region of each chip at the rear surface of said wafer; and

dicing the wafer into each chip.

2. A method of manufacturing wafer level semiconductor device comprising:

sealing the front surface of a wafer having the front and rear surfaces and having formed a plurality of semiconductor chips on the front surface thereof with resin material;

conducting electrical test to each chip;

marking in the region of each chip at the rear surface of said wafer, the position information corresponding to each chip and the result of said electrical test; and

dicing the wafer into each chip.

3. A method of manufacturing wafer level semiconductor as claimed in claim 1 or 2, wherein the circuit surface of said wafer and the opposite surface thereof are sealed with resin material and said position information and result of electrical test are marked in the region of each chip on the surface.

4. A method of manufacturing wafer level semiconductor device comprising:

sealing the front surface of a wafer having the front and rear surfaces and having formed a plurality of semiconductor chips on said front surface with resin material;

attaching a resin sheet on which marking is made on said wafer to said rear surface of wafer to indicate position of each chip; and

dicing the wafer into each chip.

5. A method of manufacturing wafer level semiconductor device as claimed in claim 4 further comprising:

conducting electrical test to each chip; and

marking the result of said electrical test corresponding to each chip to the region of each chip of the rear surface of said wafer.

6. A semiconductor device comprising:

a semiconductor chip diced from the predetermined position of wafer wherein circuits are formed at the front surface;

a resin sealing the front surface of said semiconductor chip;

an external output terminal exposed from said resin and connected with said circuits; and

a marking provided at the rear surface of said semiconductor chip to indicate the predetermined position of said wafer.

7. A semiconductor device comprising:

a semiconductor chip diced from the predetermined position of a wafer where circuits are formed at the front surface;

a resin sealing the front surface of said semiconductor chip;

an external output terminal exposed from said resin and connected to said circuit;

a resin sheet attached to the rear surface of said semiconductor chip; and

a marking indicating the predetermined position of said wafer printed on said resin sheet.